

CLAIMS

1. A memory circuit comprising:

a bit cell configured to generate a bit signal;

a sense amplifier configured to generate a reset signal  
in response to sensing said bit signal; and

5 a control circuit configured to (i) set a control latch  
in response to a detection signal and (ii) reset said control latch  
in response to said reset signal, wherein said control latch is set  
while both said detection signal and said reset signal are in an  
asserted state.

2. The memory circuit according to claim 1, further  
comprising a detection circuit configured to generate said  
detection signal in response to detecting a transition of an  
address signal.

3. The memory circuit according to claim 1, further  
comprising a pass gate configured to block said reset signal  
generated by said sense amplifier in response to said detection  
signal.

4. The memory circuit according to claim 3, further comprising a bias circuit configured to generate said reset signal in a de-asserted state to said control circuit in response to said detection signal.

5. The memory circuit according to claim 1, further comprising:

a pair of bit lines conveying said bit signal from said bit cell to said sense amplifier; and

a charging circuit configured to reset at least one of said bit lines in response to said detection signal.

6. The memory circuit according to claim 1, further comprising:

a reset latch configured to latch said reset signal as generated by said sense amplifier; and

a driver circuit configured to drive said reset latch to said de-asserted state in response to said detect signal.

7. The memory circuit according to claim 6, wherein (i) said control circuit is further configured to generate an enable

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signal in response to said detection signal and (ii) said driver  
circuit is further configured to drive said reset latch to said de-  
5 asserted state in response to said enable signal.

8. The memory circuit according to claim 1, wherein  
said sense amplifier is further configured to generate said reset  
signal in said de-asserted state in response to said detection  
signal transitioning from said asserted state to said de-asserted  
5 state.

9. The memory circuit according to claim 8, wherein  
said sense amplifier is further configured to start a new read of  
said bit cell in response to said detection signal transitioning  
from said asserted state to a de-asserted state.

10. The memory circuit according to claim 1, further  
comprising:

a pass gate configured to block said reset signal  
generated by said sense amplifier in response to said detection  
5 signal;

a bias circuit configured to generate said reset signal in a de-asserted state to said control circuit in response to said detection signal;

a pair of bit lines conveying said bit signal from said bit cell to said sense amplifier;

a charging circuit configured to reset at least one of said bit lines in response to said detection signal;

a reset latch configured to latch said reset signal as generated by said sense amplifier; and

a driver circuit configured to drive said reset latch to said de-asserted state in response to said detect signal.

11. A method of operating a memory circuit comprising the steps of:

(A) generating a bit signal;

(B) generating a reset signal in response to sensing said bit signal;

(C) setting a control latch in response to a detection signal; and

(D) resetting said control latch in response to said  
reset signal, wherein said control latch is set while both said  
10 detection signal and said reset signal are in an asserted state.

12. The method according to claim 11, further comprising  
the step of generating said detection signal in response to  
detecting a transition of an address signal.

13. The method according to claim 11, further comprising  
the step of blocking said reset signal at a first location in  
response to said detection signal.

14. The method according to claim 13, further comprising  
the step of generating said reset signal in a de-asserted state at  
a second location in response to said detection signal.

15. The method according to claim 11, further comprising  
the steps of:

conveying said bit signal in two portions from a first  
location to a second location; and

5               resetting at least one of said portions in response to  
said detection signal.

16. The method according to claim 11, further comprising  
the steps of:

5               latching said reset signal at a location; and  
                driving said reset signal to said de-asserted state at  
said location in response to said detect signal.

17. The method according to claim 16, further comprising  
the steps of:

5               generating an enable signal in response to said detection  
signal; and  
                driving said reset signal to said de-asserted state at  
said location in response to said enable signal.

18. The method according to claim 11, further comprising  
the step of generating said reset signal in said de-asserted state  
in response to said detection signal transitioning from said  
asserted state to said de-asserted state.

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19. The method according to claim 18, further comprising the step of starting a new read of said bit signal in response to said detection signal transitioning from said asserted state to a de-asserted state.

20. A memory circuit comprising:

means for generating a bit signal;

means for generating a reset signal in response to sensing said bit signal;

5 means for setting a control latch in response to a detection signal; and

means for resetting said control latch in response to said reset signal, wherein said control latch is set while both said detection signal and said reset signal are in an asserted  
10 state.